

**ABSTRACT**

In at least one hardware definition language (HDL) file, at least one design entity containing a functional portion of a digital system is specified. The design entity logically contains a configuration latch having a plurality of different possible configuration values that each corresponds to a different configuration of the functional portion of the digital system. With a statement in the HDL file(s), a Dial entity is associated with the at least one design entity. The Dial has a Dial input, a Dial output, a mapping table indicating a mapping between each of a plurality of possible input values that can be received at the Dial input and a respective corresponding output value for the Dial output, a phase ID and a default input value among the plurality of possible input values. The output value of the Dial entity controls which of the different possible configuration values is loaded in the configuration latch and the phase ID indicates a phase during which the default input value is to be applied.